WHAT IS CLAIMED IS:

1. A memory comprising: a memory cell, the memory cell including

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the source and drain regions;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

2. The memory of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer separating the polysilicon floating gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator.

3. The memory of claim 1, wherein the control gate includes a polysilicon control gate having a metal layer separating the polysilicon control gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator.

4. The memory of claim 1, wherein the gate oxide includes silicon dioxide having a tunnel barrier height of about 3.2 eV.

5. The memory of claim 1, wherein the metal oxide insulator includes a transition metal oxide.

6. The memory of claim 1, wherein the metal oxide insulator includes aluminum oxide.

7. The memory of claim 1, wherein the metal oxide insulator includes lead oxide.

8. The memory of claim 1, wherein the metal oxide insulator includes zirconium oxide.

9. The memory of claim 1, wherein the metal oxide insulator includes titanium oxide.

10. The memory of claim 1, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

11. The memory of claim 1, wherein the channel region includes an n-type channel.

12. A memory comprising: a memory cell, the memory cell including

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate;

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height;

a first metal layer separating the metal oxide insulator and the floating gate, the first metal layer in contact with the floating gate;

a second metal layer separating the metal oxide insulator and the control gate, the metal layer in contact with the control gate, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

13. The memory of claim 12, wherein the control gate is a vertical control gate.

14. The memory of claim 13, wherein the control gate is a polysilicon edge defined vertical control gate.

15. The memory of claim 12, wherein the memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

16. The memory of claim 12, wherein the metal oxide insulator includes a transition metal oxide.

17. The memory of claim 12, wherein the metal oxide insulator includes aluminum oxide.

18. The memory of claim 12, wherein the metal oxide insulator includes niobium oxide.

19. The memory of claim 12, wherein the metal oxide insulator includes tantalum oxide.

20. The memory of claim 12, wherein the floating gate includes a horizontally oriented floating gate in contact with the gate oxide.

21. The memory of claim 12, wherein the gate oxide includes silicon oxide having a tunneling barrier height of about 3.2 eV, the floating gate includes polysilicon, and the control gate includes polysilicon.

22. A memory comprising:

an array of memory cells, each memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide including silicon oxide having a tunneling barrier height of about 3.2 eV;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a tunneling barrier height less than the tunneling barrier height of the silicon oxide;

a number of bit lines coupled to the source regions along a first direction in the array of memory cells; and

a number of word lines coupled to the control gates along a second direction in the array of memory cells, wherein the memory is adapted to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

23. The memory of claim 22, wherein each memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

24. The memory of claim 22, wherein each memory cell further includes a first metal layer separating the floating gate and the metal oxide insulator, the first metal layer in contact with the metal oxide insulator, and a second metal layer separating the control gate and the metal oxide insulator, the second metal layer in contact with the metal oxide insulator.

25. The memory of claim 24, wherein the floating gate includes polysilicon, the first metal layer contacting the floating gate, and the control gate includes polysilicon, the second metal layer contacting the control gate.

26. The memory of claim 25, wherein the metal oxide insulator includes a metal oxide insulator having a tunneling barrier height of less than 2 eV.

27. The memory of claim 26, wherein the control gate is a polysilicon edge defined vertical control gate.

28. The memory of claim 25, wherein the metal oxide insulator includes a transition metal oxide.

29. The memory of claim 25, wherein the metal oxide insulator includes aluminum oxide.

30. The memory of claim 25, wherein the metal oxide insulator includes lead oxide.

31. The memory of claim 25, wherein the metal oxide insulator includes zirconium oxide.

32. The memory of claim 25, wherein the metal oxide insulator includes niobium oxide.

33. The memory of claim 25, wherein the metal oxide insulator includes tantalum oxide.

34. The memory of claim 25, wherein the metal oxide insulator includes titanium oxide.

35. The memory of claim 25, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

36. An electronic system comprising:

a processor; and

a memory coupled to the processor, wherein the memory includes an array of memory cells, each memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the source and drain regions;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height, wherein the memory is adapted to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

37. The electronic system of claim 36, wherein each memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

38. The electronic system of claim 36, wherein the control gate is a vertical control gate.

39. The electronic system of claim 36, wherein the vertical control gate is a polysilicon edge defined vertical control gate.

40. The electronic system of claim 36, wherein the gate oxide includes silicon oxide having a tunneling barrier height of about 3.2 eV.

41. The electronic system of claim 36, wherein the metal oxide insulator includes a transition metal oxide.

42. The electronic system of claim 36, wherein the metal oxide insulator includes aluminum oxide.

43. The electronic system of claim 36, wherein the metal oxide insulator includes lead oxide.

44. The electronic system of claim 36, wherein the metal oxide insulator includes tantalum oxide.

45. The electronic system of claim 36, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

46. An electronic system comprising:

a processor; and

a memory coupled to the processor, wherein the memory includes:

an array of memory cells, each memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate;

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height; and

a first metal layer separating the floating gate and the metal oxide insulator, the first metal layer in contact with the metal oxide insulator;

a number of bit lines coupled to the source regions along a first direction in the array of memory cells; and

a number of word lines coupled to the control gates along a second direction in the array of memory cells, wherein the memory is adapted to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

47. The electronic system of claim 46, wherein each memory cell further includes a second metal layer separating the control gate and the metal oxide insulator, the second metal layer in contact with the metal oxide insulator.

48. The electronic system of claim 47, wherein the floating gate includes polysilicon, the first metal layer contacting the floating gate, and the control gate includes polysilicon, the second metal layer contacting the control gate.

49. The electronic system of claim 48, wherein the gate oxide includes silicon oxide having a tunneling barrier height of about 3.2 eV.

50. The electronic system of claim 49, wherein the metal oxide insulator includes zirconium oxide.

51. The electronic system of claim 50, wherein the metal oxide insulator includes a transition metal oxide.

52. The electronic system of claim 50, wherein the metal oxide insulator includes zirconium oxide.

53. The electronic system of claim 50, wherein the metal oxide insulator includes niobium oxide.

54. The electronic system of claim 50, wherein the metal oxide insulator includes titanium oxide

55. The electronic system of claim 50, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

56. A method of forming a memory, comprising:

forming a memory cell including:

forming a source region and a drain region separated by a channel region in a substrate;

forming a storage capacitor coupled to one of the source and drain regions;

forming a gate oxide on the channel region, the gate oxide having a first tunneling barrier height;

forming a floating gate opposing the channel region, the floating gate separated from the channel region by the gate oxide;

forming a control gate opposing the floating gate; and

forming a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier

height, the second tunneling barrier height being less than the first tunneling barrier height; and

adapting the memory to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

57. The method of claim 56, wherein forming a metal oxide insulator includes forming a transition metal oxide insulator.

58. The method of claim 56, wherein forming a metal oxide insulator includes forming aluminum oxide.

59. The method of claim 56, wherein forming a metal oxide insulator includes forming zirconium oxide.

60. The method of claim 56, wherein forming a metal oxide insulator includes forming lead oxide.

61. The method of claim 56, wherein forming a metal oxide insulator includes forming a Perovskite metal oxide insulator.

62. The method of claim 56, wherein forming a floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the metal oxide insulator.

63. The method of claim 56, wherein forming a control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the metal oxide insulator.

64. The method of claim 56, wherein forming a gate oxide includes forming silicon dioxide having a tunneling barrier height of about 3.2 eV.

65. The method of claim 56, wherein forming a control gate includes forming an edge defined vertical control gate.

66. A method of forming a memory, comprising:

forming an array of memory cells, wherein forming each memory cell includes:

forming a source region and a drain region separated by a channel region in a substrate;

forming a storage capacitor coupled to the drain region;

forming a floating gate opposing the channel region;

forming a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

forming a first metal layer on the floating gate, the first metal layer in contact with the metal oxide insulator;

forming a control gate opposing the floating gate; and

forming a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height;

forming a number of bit lines coupled to the source regions along a first direction in the array of memory cells;

a number of word lines coupled to the control gates along a second direction in the array of memory cells; and

adapting the memory to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

67. The method of claim 66, wherein adapting the memory to operate each memory cell includes adapting the memory to control each memory cell to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode, wherein the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

68. The method of claim 66, wherein the method further includes forming a second metal layer on the control gate, the second metal layer in contact with the metal oxide insulator.

69. The method of claim 68, wherein forming a floating gate includes forming a polysilicon floating gate.

70. The method of claim 69, wherein forming a gate oxide includes forming silicon oxide having a tunneling barrier height of about 3.2 eV.

71. The method of claim 70, wherein forming a metal oxide insulator includes forming a transition metal oxide.

72. The method of claim 70, wherein forming a metal oxide insulator includes forming titanium oxide.

73. The method of claim 70, wherein forming a metal oxide insulator includes forming tantalum oxide.

74. The method of claim 70, wherein forming a metal oxide insulator includes forming niobium oxide.

75. The method of claim 70, wherein forming a metal oxide insulator includes forming a Perovskite metal oxide insulator.

76. The method of claim 70, wherein forming a source region and a drain region includes forming a n+ source region and a n+ drain region.

77. The method of claim 70, wherein the forming a control gate lines includes forming a forming a vertical control gate.

78. The method of claim 70, wherein the forming a control gate lines includes forming a forming an edge defined vertical control gate.

79. A method of forming an electronic system, comprising:

providing a processor; and

coupling the processor to a memory, the memory formed by a method including:

forming a memory cell, the memory cell formed by:

forming a source region and a drain region separated by a channel region in a substrate;

forming a storage capacitor coupled to one of the source and drain regions;

forming a gate oxide on the channel region, the gate oxide having a first tunneling barrier height;

forming a floating gate opposing the channel region, the floating gate separated from the channel region by the gate oxide;

forming a control gate opposing the floating gate; and

forming a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height; and

adapting the memory to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

80. The method of claim 79, wherein adapting the memory to operate the memory cell includes adapting the memory to control the memory cell to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode, wherein the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

81. The method of claim 79, wherein the method further includes forming a first metal layer on the floating gate, the first metal layer in contact with the metal oxide insulator.

82. The method of claim 81, wherein forming a gate oxide includes forming silicon dioxide having a tunneling barrier height of about 3.2 eV.

83. The method of claim 82, wherein forming a floating oxide includes forming a polysilicon floating gate and forming a control gate includes forming a polysilicon control gate.

84. The method of claim 81, wherein the method further includes forming a second metal layer on the control gate, the second metal layer in contact with the metal oxide insulator.

85. The method of claim 81, wherein forming a metal oxide insulator includes forming a transition metal oxide insulator.

86. The method of claim 81, wherein forming a metal oxide insulator includes forming aluminum oxide.

87. The method of claim 81, wherein forming a metal oxide insulator includes forming zirconium oxide.

88. The method of claim 81, wherein forming a metal oxide insulator includes forming lead oxide.

89. The method of claim 81, wherein forming a metal oxide insulator includes forming a Perovskite metal oxide insulator.

90. A method comprising:

operating a memory adapted to control a memory cell in a volatile memory mode and in a non-volatile memory mode, the memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the source and drain regions;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height;

sensing a first charge representing a data value from the storage capacitor if the memory operates the memory cell in the volatile memory mode; and

sensing a second charge representing a data value from the floating gate if the memory operates the memory cell in the volatile memory mode.

91. The method of claim 90, wherein the method further includes writing to the floating gate using channel hot electron injection.

92. The method of claim 91, wherein writing to the floating gate using channel hot electron injection includes:

applying a large voltage to the control gate; and

applying a large voltage to the drain region.

93. The method of claim 90, wherein the method further includes writing to the floating gate by tunneling electrons from the control gate to the floating gate.

94. The method of claim 93, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate includes:

applying a positive voltage to the substrate; and

applying a large negative voltage to the control gate.

95. The method of claim 90, wherein the method further includes erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate.

96. The method of claim 95, wherein erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate includes:

providing a negative voltage to the substrate; and

providing a large positive voltage to the control gate.

97. The method of claim 95, wherein tunneling electrons from the floating gate to the control gate includes tunneling electrons from a first metal layer formed on the floating gate through the metal oxide insulator to a second metal layer formed on the control gate, the first metal layer in contact with the metal oxide insulator and the second metal layer in contact with the metal oxide insulator.

98. The method of claim 90, wherein the method further includes reading the memory cell in the non-volatile memory mode by:

applying a positive voltage to the control gate of the memory cell; and

sensing a current from the drain region.

99. The method of claim 90, wherein operating the memory to control the memory cell in the volatile memory mode includes reading charge from the capacitor of the memory cell and/or writing charge from the capacitor of the memory cell.

100. A method comprising:

operating a memory adapted to control a memory cell in a volatile memory mode and in a non-volatile memory mode, the memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a polysilicon floating gate opposing the channel region, the polysilicon floating gate having a metal layer disposed thereon;

a silicon oxide layer separating the floating gate from the channel region, the silicon oxide layer having a tunneling barrier height of about 3.2 eV;

a metal oxide insulator, the metal oxide insulator having a tunneling barrier height being less than the tunneling barrier height of the silicon oxide layer, the metal oxide insulator in contact with the metal layer disposed on the polysilicon floating gate; and

a control gate opposing the floating gate and separated from the floating gate by the metal oxide insulator; and

sensing a first charge representing a data value from the storage capacitor if the memory operates the memory cell in the volatile memory mode; and

sensing a second charge representing a data value from the floating gate if the memory operates the memory cell in the volatile memory mode.

101. The method of claim 100, wherein the method further includes writing to the floating gate using channel hot electron injection.

102. The method of claim 101, wherein writing to the floating gate using channel hot electron injection includes:

applying a large voltage to the control gate; and

applying a large voltage to the drain region.

103. The method of claim 100, wherein the method further includes writing to the floating gate by tunneling electrons from the control gate to the floating gate.

104. The method of claim 103, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate includes:

applying a positive voltage to the substrate; and

applying a large negative voltage to the control gate.

105. The method of claim 100, wherein the method further includes erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate.

106. The method of claim 105, wherein erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate includes:

providing a negative voltage to the substrate; and

providing a large positive voltage to the control gate.

107. The method of claim 105, wherein tunneling electrons from the floating gate to the control gate includes tunneling electrons from the metal layer disposed on the floating gate through the metal oxide insulator to a metal layer disposed on the control gate, the metal layer disposed on the control gate in contact with the metal oxide insulator, the control gate including polysilicon.

108. The method of claim 100, wherein the method further includes reading the memory cell in the non-volatile memory mode by:

applying a positive voltage to the control gate of the memory cell; and

sensing a current from the drain region.

109. The method of claim 100, wherein operating the memory to control the memory cell in the volatile memory mode includes reading charge from the capacitor of the memory cell and/or writing charge from the capacitor of the memory cell.

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